REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-18 were pending and rejected. In this response, no claim has been canceled. Claims 1-16 have been amended. In addition, new claims 19-27 have been added. Thus, claims 1-27 remain pending. No new matter has been added.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,216,178 of Stracovsky et al. ("Stracovsky") in view of U.S. Patent No. 6,128,702 of Saulsbury ("Saulsbury"). In view of the foregoing amendments, it is respectfully submitted that claims 1-27 are patentable over the cited references. Specifically, independent claim 1 as amended recites as follows:

> 1. A memory controller, comprising:
>
> a plurality of tag units, each tag unit including an array of tag address storage locations, the plurality of tag units to perform tag look-up operations in response a memory access request;
>
> a memory module decode unit, the memory module decode unit to perform decode operations to determine which one of a plurality of memory modules is being accessed by the memory access request substantially concurrently with respect to the tag look-up operations; and
>
> a command sequencer and serializer unit coupled to the array of tag address storage locations and the memory module decode unit, the command sequencer and serializer unit to serialize commands and address information and sequentially transmit, over a serial link of a memory bus coupling the memory control with a plurality of memory modules, to a memory module to access a data cache located on the memory module that is specified by the memory module decode unit as a result of the decode operations, if the lookup operations indicate that at least one of the tag addresses matches a memory address of the memory access request.
>
> (Emphasis added)

Independent claim 1 includes a memory controller having multiple tag units and each tag unit includes an array of tag address storage location, where each tag unit performs a lookup operation to determine whether there is a cache hit for a memory access request.

In addition, the memory controller includes a memory module decode unit performs decode operations to determine which of the memory modules is being accessed substantially concurrently. As result, by the time when the lookup operations have been performed to determine whether there is a cache hit, the memory controller already knows which of the memory modules is being accessed.

Furthermore, the memory controller includes a command sequencer and serializer unit to serialize the commands and address information and sequentially transmit this information to the determined memory module over a serial link of a memory bus, such as, for example, a point-to-point interconnected as recited in claims 9 and 22-23. It is respectfully submitted that the above limitations are absent from the cited references.

Rather, Stracovsky is related to a conventional memory controller for memory access. However, Stracovsky fails to disclose multiple tag unit performing lookup operations substantially concurrently with a memory module decode unit, where a command sequencer and serializer unit access a cache of a memory module determined by the memory module decode unit based on whether there is a cache hit determined by the tag units.

The Examiner contends that section col. 6, line 21 to col. 7, line 10 of Stracovsky reads on the above limitation (see, 3/25/2004 Office Action, page 3). Applicant

respectfully disagrees. The cited section basically describes Fig. 1B of Stracovsky, where nowhere in Figure 1B shows the above limitations.

Further, it is respectfully submitted that Stracovsky also fails to disclose a command sequencer and serializer serializes the command and address information and sequentially transmits the information over one or more serial links of a memory bus, such as, for example, via a point-to-point interconnect as recited in claims 9 and 22-23, to a determined memory module.

The Examiner contends that Figure 9 and col. 11, line 50 to col. 13, line 4 of Stracovsky discloses the point-to-point interconnect as claimed in the present invention (see, see, 3/25/2004 Office Action, page 4). Applicant respectfully disagrees. A point-to-point interconnect has a specific meaning in the industry and typically a serial communication from a point to another point. It is respectfully submitted that Stracovsky fails to disclose or suggest such a limitation. In fact, there is mention of a point-to-point interconnect in Stracovsky.

Although the Examiner acknowledged that Stracovsky fails to disclose access a cache memory located on a memory module, the Examiner maintained that Saulsbury discloses such a limitation. Although, Saulsbury discloses a cache memory on a memory module, however, such an application is significantly different from Saulsbury and the present invention as claimed.

Saulsbury is related to an integrated processor/memory device where a memory controller is intended to be eliminated. It is respectfully submitted that there is no suggestion within Saulsbury and Stracovsky to combine with each other. As described above, the primary purpose of Saulsbury is to eliminate a memory controller by

integrating the memory with a microprocessor, while Stracovsky emphasizes a universal controller that can be used in a variety of system configurations. It appears that they teach away from each other. It is respectfully submitted that one with ordinary skill in the art would not, based on the teaching of Saulsbury and Stracovsky, to combine these two references because it lacks a reasonable expectation of success. Even if they were combined, such a combination still lacks the limitations set forth above. Therefore, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claims 10 and 16 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, independent claims 10 and 16 are patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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